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Feature Articles: Superconducting Digital Device
- Trends of Superconducting Digital Device Technology

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Logic circuits or integrated circuits that exploit Josephson Junctions for superconducting digital applications have a 40-year history. The events marking the historical evolution seem to occur every 20-years, with the present time representing the transition period from the second to the third generation. The first-generation encompassed latching logic circuits, which evolved to a second-generation single flux quantum logic circuit (RSFQ circuit). The present third-generation involves a low-energy consumption SFQ circuit.

Figure 1 represents the evolutionary relationship between the bit-energy and the clock period for relatively large-scale integrated circuits such as the microprocessor fabricated up to now. Here, the bit-energy is defined as the power consumed per clock period divided by the number of active devices like Josephson junctions. The clock period and bit-energy for both the semiconductor CMOS device and the first-generation latching circuits are already at similar values. However, considering the additional costs associated with cryocooling made the CMOS circuit far more attractive than the latching circuit.

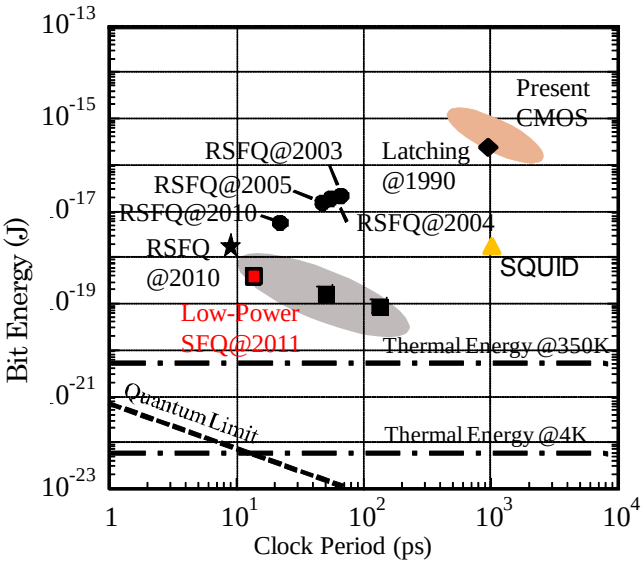

Fig. 1 Evolutionary relationship between the bit energy and clock period for each type of integrated circuit

It was the RSFQ circuit design that significantly changed this state of affairs. Employing the same fabrication process, the clock period and bit-energy were reduced by more than one order of magnitude. Furthermore, the advanced process (ADP) developed at ISTEC demonstrated the possibility of circuits exceeding 100GHz operational frequency. This has reduced the bit-energy by one further order. Figure 2 is a complex co-processor prototype fabricated with the ADP, designed specially for scientific computation. The circuit consisting of a total of 11458 Josephson Junctions operated at 45GHz, with a power consumption of 3.4mW. The products of the operating frequency and the

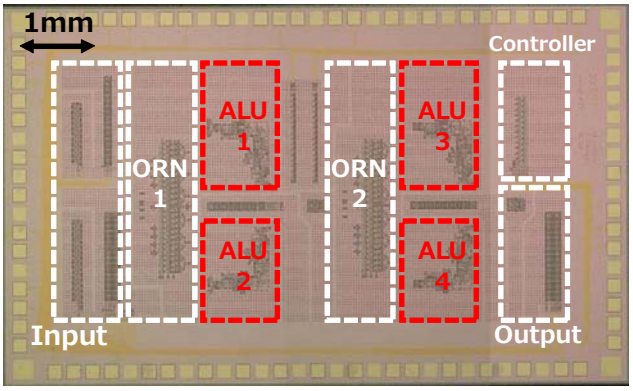

Fig. 2 A micrograph of a co-processor prototype fabricated with the ADP, designed specially for scientific computation

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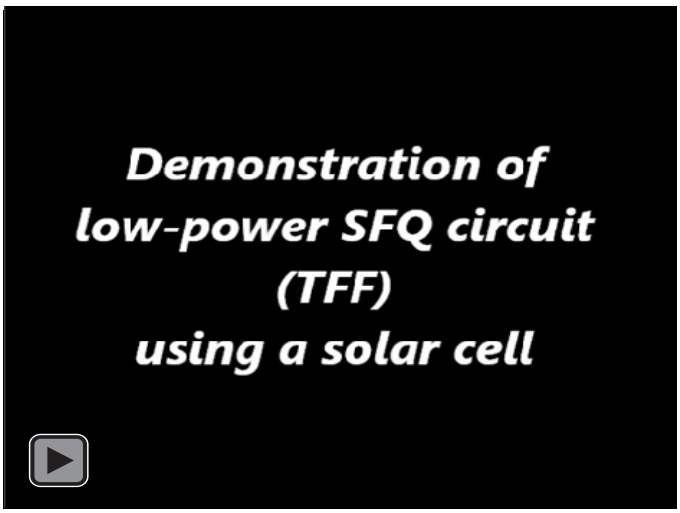
bit-energy of current RSFQ circuits have an overall 4 orders of magnitude less than those of the semiconductor CMOS counterparts, offering superior performance even taking into account the additional costs associated with cryocooling. The movie demonstrates a toggle flip-flop (TFF) using a solar cell and clearly shows the superiority of the SFQ circuit fabricated with ADP. The system operates up to 288GHz and consumes less than 15μW of power. Apart from future IT equipment-related applications, the development of this SFQ circuit has been proactively advancing for superconducting detector system applications. The system operates by detecting the power output from a multi-element detector, which after signal processing is multiplexed to room-temperature electronics. In Japan, the developments in a single photon detector, neutron detector and a mass spectrometer have been undertaken.



The demonstration of a low-power SFQ circuit (toggle flip-flop (TFF)) using a solar cell (Movie)

Nevertheless the limit is in sight, and performance enhancements of semiconductors have continued. Considering this present situation, a performance improvement of more than one order is desired in order to assure the superiority for the future of superconducting digital circuits. Conventional RSFQ circuits consume 90% of their energy at the current-limiting resistors. Therefore, the proposal is to reduce the power consumption at these current-limiting resistors. Current limiting resistors are placed between the voltage source and the Josephson junction to determine the current flowing into the Josephson junction. A relatively large resistance is required for driving Josephson junctions in a constant-current mode, resulting in increased power consumption. In the USA, methods specifically designed to reduce power consumption have been explored, and include reducing the AC-driven current by adjusting the ratio of the transformer windings and replacing the current-limiting resistor with an inductor and a Josephson junction. In Japan, at the Yokohama National University and Nagoya University, the current-limiting resistance value has been reduced to around 1/10 the original value by adopting an LR-biasing technique of placing the inductance in series with the resistance.

Recent attempts have been made to reduce the power consumption of Josephson junctions. The basic idea is to suppress voltage generation by delaying the switching time of the Josephson Junctions. nSQUID, developed by Stony Brook University, adiabatic-type QFT developed by Yokohama National University, and the low-voltage RSFQ developed by Nagoya University are examples of this idea. Further to the relationship between the bit-energy and clock period, the experimental values obtained are plotted as

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Low-Power SFQ in Figure 1. It shows that although the operating speed is slower, the bit-energy is significantly reduced with the product of the bit-energy and the clock period being more than five orders of magnitude superior to an semiconductor circuit counterpart. The energy consumption of Josephson junctions itself has already become less than conventional SQUIDs. nSQUID and adiabatic-type QFP are considered possible to reduce bit-energies up to both the thermodynamic and quantum mechanical limitations. Future development is highly expected.

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