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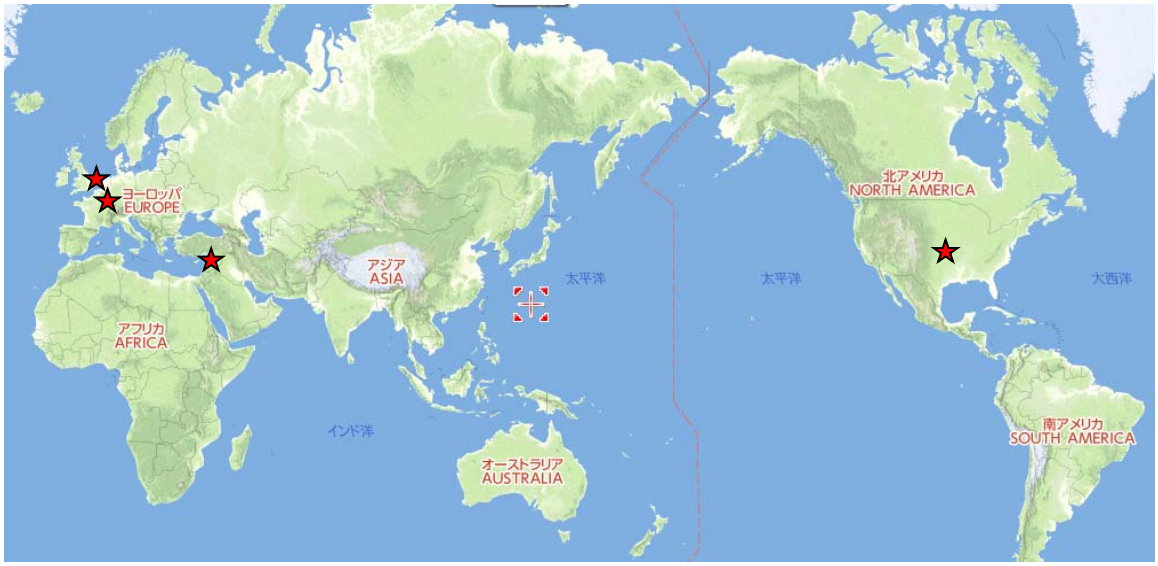
What's New in the World of Superconductivity (November, 2013)

초전도 뉴스 –세계의 동향–

超导新闻 –世界的动向-

chāo dǎo xīnwén - shìjiè de dòngxiàng-

Yutaka Yamada, Principal Research Fellow
Superconductivity Research Laboratory, ISTEC



★News sources and related areas in this issue

▸Electronics 엘렉트로닉스 电子应用［diànzǐyè yìngyòng]

Super SQUID

Weizmann Institute of Science (November 25, 2013)

Scientists at the Weizmann Institute of Science have created the world's smallest SQUID (superconducting quantum interference device), breaking the world record for sensitivity and resolution in the measurement of magnetic fields. Nano-SQUIDs can be placed on probes and used to scan and measure the magnetic field at different points on a sample; the resulting data can then be combined to form an image of the entire surface. The scientists at the Weizmann Institute used a hollow quartz tube and pulled it into a very sharp

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point. They then fabricated a SQUID with a diameter of only 46 nm that encircled the tip of the pointed tube. A scanning microscope was then constructed around the tip. Using this set-up, the group was able to obtain magnetic images at distances as small as a few nanometers from the sample. PhD student Lior Embon commented, “While there are SQUIDs with higher sensitivities to uniform magnetic fields, the combination of high sensitivity, proximity of the probe to the sample and its minute dimensions make the overall accuracy of the device record-breaking." The group’s results have been reported in *Nature Nanotechnology*.

Source: “Super SQUID”
Weizmann Institute of Science press release (November 25, 2013)
URL: http://wis-wander.weizmann.ac.il/super-squid#.Urk2b_RSYSE
Contact: news@weizmann.ac.il

▸Basics 기초 基础[jīchǔ]

Doubt on Origin of High-temperature Superconductivity

Institut Laue-Langevin (November19, 2013)

Researchers at the Institut Laue-Langevin (ILL; Grenoble, France) have published a paper in *Nature Communications* describing an ‘hourglass’ magnetic excitation spectrum in a fluctuating charge stripe-less cobaltate compound, thereby suggesting that the evidence for fluctuating charge stripes being a candidate for the explanation of high-temperature superconductivity is not compelling. Charge stripes are created during material doping to create a ‘charge reservoir’ in superconductors, creating holes that have a tendency to organize themselves into stripes. While static stripes have been directly observed, the stripes are difficult to observe when fluctuating, and it is these fluctuations that have been thought to play a role in high-temperature superconductivity. These charge stripes are typically accompanied by a very specific magnetic excitation spectrum known as an ‘hourglass’ spectrum, which is a hallmark of high-temperature superconductors. To investigate this relationship, researchers from the Max-Planck Institute (Dresden, Germany) working at ILL and LLB in Saclay have been studying the magnetism, magnetic excitations, charge ordering, and electron-phonon coupling in a stripeless single-layer perovskite colbatate compound. The lack of stripes in this compound was expected to result in the absence of an hourglass spectrum. However, a familiar magnetic excitation spectrum with all the basic features of an hourglass spectrum was, indeed, observed, ruling out the possibility of a link between stripes and a hourglass spectrum in the presently examined cobaltate material. In addition to cautioning researchers regarding the stripe theory of superconductivity, the group also obtained evidence supporting alternative causes of the hourglass excitations, such as a magnetic effect known as frustration (in which atoms within the crystal lattice are prevented from aligning with each other because of conflicting demands from neighboring atoms).

Source: “Neutrons cast serious doubt on major ‘suspect’ in search for origins of high-temperature superconductivity”

Institut Laue-Langevin press release (November 2013)
URL:
http://www.ill.eu/news-events/press-room/press-releases/neutrons-cast-serious-doubt-on-major-suspect-in-search-for-origin-of-high-temperature-superconductivity-november-2013/
Contact: Dr Andrea Piovano, piovano@ill.fr

New Hydrogen-storing Material (Iridium Hydride)

Deutsches Elektronen-Synchrotron (November 20, 2013)

An international group performing high-pressure X-ray studies at Deutsches Elektronen-Synchrotron (DESY) has detected the formation of previously unobserved iridium hydride synthesized from hydrogen and metallic iridium at a pressure of 55 GPa. This new material can store up to three times more hydrogen than most other metal hydrides, potentially contributing to the development of high-capacity hydrogen fuel cells in cars and other applications. The new material has an unexpected structure that does not occur in other known hydrides, potentially leading to the discovery of unprecedented properties. In addition, metal hydrides could act as superconductors; such behavior has been observed or predicted for hydrides of noble metals such as palladium and platinum and might also occur in hydrides of other chemically related noble metals, such as iridium. The new material was fabricated by placing a piece of iridium inside a pressure cell (known as a diamond anvil cell) and then loading the cell with hydrogen. The sample was then compressed using pressures as high as 125 GPa. Simultaneously, intense and bundled X-rays were applied to the sample, revealing its structural changes accompanying variations in pressure. In this manner, an iridium trihydride phase than can store up to three times more hydrogen than most other metal hydrides was observed. Future research is expected to examine the material's mechanical and electronic properties. The group's work has been published in *Physical Review Letters*.

Source: "Novel material stores unusually large amounts of hydrogen"
Deutsches Elektronen-Synchrotron press release (November 20, 2013)
URL: http://www.desy.de/information__services/press/pressreleases/@@news-view?id=6701
Contact: desyinfo@desy.de

▸Management and Finance 경영정보 经营信息[jīngyíng xìnxī]

Financial Report and Wire Perspective

Superconductor Technologies Inc. (November 12, 2013)

Superconductor Technologies, Inc. (STI), has reported its financial results for the third quarter ending September 28, 2013. The third quarter net revenues totaled USD $229,000, while the net loss was $3.5

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million. As of September 28, 2013, STI had $10.3 million in cash and cash equivalents. Jeff Quiram, STI's president and chief executive officer, commented, "In the third quarter, we advanced our progress in commercializing our Conductus® wire by fully completing our first purchase order, continuing to ship against other existing orders, and further increasing our order pipeline. Current shipments of Conductus wire are for qualification testing for our target superconducting applications, including fault current limiters, high-field magnets, industrial motors and generators, and power transmission cables… Due to the strong market interest in our wire, customer demand continues to create a backlog of orders for qualification testing. We expect these current commitments will consume all the wire we can produce for at least the next three months. Our objective over the next several months is to secure orders for our planned 2014 production." The company has also begun receiving the delivery of various components for a 1-kilometer RCE machine. The completion of all deliveries required for the assembly of the device is expected to occur in the first quarter of 2014. The company expects to exit the second quarter of next year with significant wire production capacity that should enable a positive cash flow from operations in the second half of 2014.

Source: “Superconductor Technologies Reports Third Quarter 2013 Results”
Superconductor Technologies Inc. press release (November 12, 2013)
URL: http://phx.corporate-ir.net/phoenix.zhtml?c=70847&p=irol-newsArticle&ID=1875150&highlight
Contact: Investor Relations, Cathy Mattison or Becky Herrick of LHA for Superconductor Technologies Inc., invest@suptech.com, ; HTS Wire, Mike Beaumont of STI, mbeaumont@suptech.com

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Feature Article: Superconducting Digital Devices - Expectations of A Supercomputer and Data Center Employing Superconducting Devices

Akira Fujimaki, Professor
Graduate School of Engineering
Nagoya University

Currently there is rapid momentum behind a vision to construct a supercomputer and data center that utilizes superconducting devices. The impetus has arisen at the launch of the Cryogenic Computing Complexity (C3) program held in USA, which has conducted an in-depth feasibility study spanning several years. The program targets computing performance that otherwise could not be realized using conventional CMOS semiconductor technology. This article briefly summarizes the current status of microprocessor and memory development forming the foundation of the C3 program proposals, along with a foresight into future prospects.

As highlighted by the author's article published in Superconductivity Web21 last year, superconducting digital circuits have undergone reviews of circuit configuration methods addressing areas such as reducing power consumption and increasing energy efficiencies. The results from such studies have today yielded the confirmation of superconducting integrated circuits having 1-2 digit greater efficiencies compared to conventional semiconductor integrated circuits, even when taking into account cryocooling penalties. The active element or Josephson Junction has been the driving force behind the conventional Rapid Single Flux Quantum (RSFQ) circuit acting as the current source. A current-limiting resistor exhibiting a resistance greater than the Josephson Junction impedance was therefore required and sandwiched between the power supply and Josephson Junction. Despite this, there was difficulty using this method that prevented the realization of higher efficiencies because of the power consumed by this current-limiting resistor, i.e. the static power consumption was far greater than the dynamic power consumed by the Josephson Junction itself. The current circuit methodologies proposed are proving successful in significantly reducing or completely eliminating static power consumption.

Nagoya University has now proposed low voltage RSFQ circuits that enable the realization of lower power consumption in a relatively simple way. The proposals aim to minimize both the power supply voltage and current limiting resistance to between $1/5^{th}$ and$1/10^{th}$ of a conventional RSFQ circuit. Table 1 shows the summary performance characteristics of a superconducting microprocessor developed thus far as well as a microprocessor in the middle of development. The performance attributes of a current CMOS semiconductor-based microprocessor are also noted. The power efficiency of the superconducting microprocessor, an important performance indicator, has already been measured to be 1700 giga operations/W (GOPS/W) by employing low voltage RSFQ CORE processors, which is 4000-times superior compared to CMOS. This indicates the microprocessor to be around 1-digit superior, even taking into account the power consumption of the cooler. The author considers that future higher integration and architecture optimization will bring over 2-digit superiority compared to a semiconductor-based microprocessor. Although the USA does not have a track record to be able to verify the superconducting

microprocessor performance characteristics up to now, rapid development is anticipated towards the performance targets included in C3 program as shown in Table 1.

Table 1 Performance index of a superconducting microprocessor

	CORE1a-ver5	LV-RSFQ CORE	LV-RSFQ RISC	C3	CMOS
Verification year (including plan)	2003	2013	2017	2020	2013
System clock frequency	1 GHz	2 GHz	3 GHz	10 GHz	2 GHz
Word length	8 bit	8 bit	32 bit	64 bit	64 bit
Data format	bit serial	bit serial	bit slice	paralell	paralell
Power efficiency	100 GOPS/W	1700 GOPS/W	4000 GOPS/W	-	0.04 GOPS/W

A high-speed, high capacity memory is a prerequisite in the construction of a supercomputer and data center. An essential route to realize greater speeds or reduce access times is to minimize the physical size of the memory cell unit. However, since the fundamental concept of conventional memory is to store flux quanta, a superconducting loop is required no matter what. This physically increases the memory cell size. An additional issue with conventional memory is the relatively large energy consumption during input/output flux quanta. To address this, a concept of a superconducting magnetic memory (MRAM) has been proposed with the research mainly led in the USA. Superconducting MRAMs, similar to ordinary MRAMs, employ magnetic thin films between tunnel junctions allowing the storage of two values of information dependent upon the magnetization direction. Having the memory being made up of a single-unit magnetic junction reduces the cell size and higher speed gains are thus expected. Also, as flux quanta are not required this leads to potentially reducing power consumption. The C3 program includes the development for such a new memory, with the final aims being greater speeds and larger memory capacities. However, essential to the operations of superconducting MRAMs are read-out and write-in operations, which have yet to be verified at present. The degree of usability will be determined on the progress of future research outcomes.

As mentioned by this article, superconducting digital circuits are somewhat undergoing a revolution in their use for large-scale computing systems. It was challenges with latch circuits during the 1970s and RSFQ circuits during the 1990s in the USA, but now the third set of challenges are producing high-energy efficient single flux quantum circuits. It is therefore important for Japan to step up to the mark to address this challenge to cooperate in this venture by making use of Japan's superior technological prowess in process and design technology.

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Feature Article: Superconducting Digital Devices - Achievements and Issues with CREST (Low Power, High-Performance, Reconfigurable-Processors Employing Single Flux Quantum Circuits)

Naofumi Takagi, Professor
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Kyoto University

Superconducting Single Flux Quantum (SFQ) circuits are predicted to offer a combination of ultra-high speeds and ultra-low power-consuming circuits not attainable using current semiconductor technology. The author and his group have focused their research on “low power, high performance reconfigurable -processors utilizing single flux quantum circuits,” under the JST-CREST program, which took place between October 2006 and March 2013. (Please refer to the author’s article “Present Status of Research and Development in Low-power, High-performance Processors Employing SFQ Circuits”, which appeared in the October 2009 issue of Superconductivity Web 21.) Engaging SFQ circuits will allow the realization of Reconfigurable Data Paths (RDP) composed of several-thousands of Floating Point Units (FPU) and a network (ORN) connecting them. These could be coupled to an ordinary processor to act as a computation accelerator. ORN is reconfigured according to a series of iterative computation loops, which typically appear in large-scale computations. Greater computing performance is to be realized with a large number of FPUs operating in parallel. The project aims were to establish fundamental RDP technology employing SFQ circuits, in a joint research venture between Kyoto University, Kyushu University, Yokohama National University, Nagoya University and the Superconductivity Research Laboratory. The research activities have included SFQ circuit processing, SFQ operating circuits, reconfiguration mechanisms and RDP architecture technology.

The processing of SFQ circuits have led to the development of fully planarization technology leading to the establishment of a Nb 9-layer 1μm fabrication process exhibiting 2-layer Passive Transmission Line (PTL). In addition to the construction of the logic cell library, a series of circuit design supporting tools have also been developed. Circuit technology that consumes very little power has also been developed. A Floating Point Adder, Floating-Point Multiplier (FPM), divider, and square-root circuit configurations have been developed as part of the SFQ circuit, enabling the successful operational verification of half-precision FPA and FPM operating at more than 60 GHz. The successful operation of a prototype ORN functioning up to 45 GHz has been verified with the employment of the ORN configuration consisting of a crossbar multi-stage interconnection network required as part of the reconfiguration mechanism. Furthermore, a prototype RDP has been developed with a 2x2 RDP and its operations successfully verified at 45 GHz. Although the complete operational verification of 4x4 RDP (picture) was originally set as the final target, it has not yet been achieved, however, a configuration mechanism up to 3x3 has been confirmed. RDP technology architecture has advanced from both the viewpoints of application analysis and feasibility studies utilizing SFQ circuits. A detailed architecture of RDP has been determined based upon the analysis of an array of scientific computations. An RDP evaluation tool has also been fabricated together with an RDP compiler. An algorithm for the RDP has been developed to cope with a number of numeric computations such as heat conduction equations. These results have hinted at the possibility of designing

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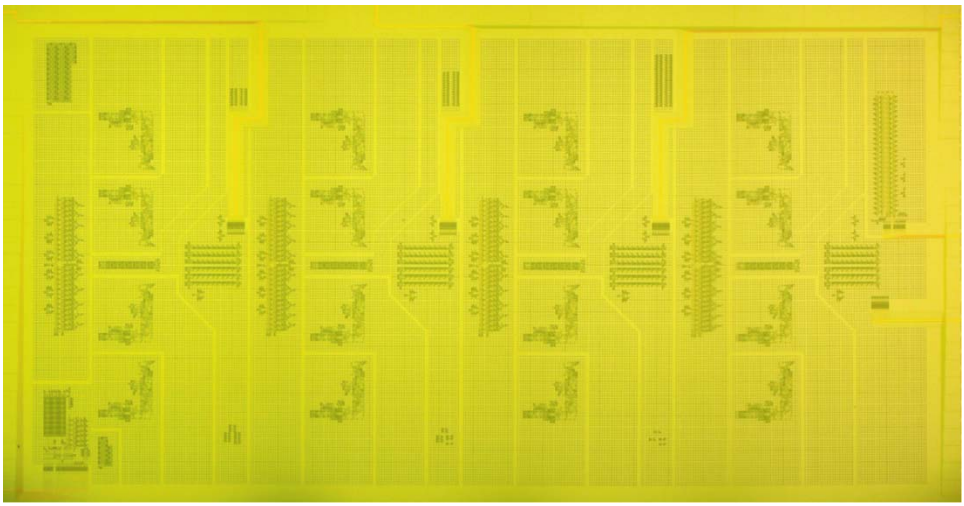
and fabricating large-scale SFQ circuits along with the potential offered by SFQ-RDPs, increasing the effectiveness of some scientific computations. Moreover, the performance assessments of SFQ circuits produced using a 0.5 μm fabrication process has alluded to the possibility of potential SFQ-RDPs operating at 10 teraflops and only consuming 3.2 W of power.

The research targets have mostly been achieved. In particular, the development of world-leading process technologies, device technologies and logic design technologies has led to the fabrication of the world's largest prototype circuit, the operational performance of which has been verified and can be considered as proud achievements. Nonetheless, a prototype 4x4 RDP composed of a 16-unit ALU consisting of several-thousands of FPUs is far from realization of a practical RDP. It still remains that an RDP is applicable for use in an SFQ circuit. Coupling an SFQ-RDP with an ordinary processor to serve as a computational accelerator does not require superconducting memory. Thus, it is relatively easy to realize. However, there is a risk that the main memory bandwidth and the bandwidth of data interchange with RDP could limit system performance. Here, providing ultra-high speed memory at the accelerator side and the installation of a streaming buffer to interchange data with the RDP are areas that requires further investigations. Since RDPs applicable to scientific computations are limited, the future development of superconducting memory is desired together with an exploration of effective architecture allowing the realization of SFQ circuits pertinent to a variety of scientific computations.

This project has led to the development of planarization technology and PTL multi-layer fabrication technology. The author considers that around 0.2 μm-sized SFQ circuits can be realized without any issues by employing already existing processing technology designed for semiconductor integrated circuits. Enhancing device performance is desired in future research studies.



Picture: A prototype 4x4 RDP LSI fabricated utilizing 1 μm SFQ processing
Four-rows of four ALUs, where each ALU in close proximity is connected via ORN. Die size is 11.0 mm x 5.5 mm; 28,528 Josephson Junctions

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Feature Article: Superconducting Digital Devices -Likelihood of Adiabatic QFP Logic Circuits and Reversible Computing

Nobuyuki Yoshikawa, Professor
Graduate School of Engineering
Yokohama National University

The performance characteristics of high-end information equipment are currently limited by power consumption, and it is therefore necessary to drastically reduce the power consumed by logic circuits to enhance future performance. Superconducting integrated circuit technology is anticipated to allow greater energy efficiencies far exceeding those of semiconductor-based circuits. It has been mainly Japan and the USA that have led projects aimed at realizing information equipment that consumes lower powers[1), 2)]. Recent years has seen several proposals related to new circuit configurations that consume very little power by utilizing superconducting digital integrated circuits, with vigorous research and development activities undertaken in this area [3)].

Fundamentally lowering power consumption in logic circuits requires reducing the energy consumed per bit. Conventional CMOS and Single Flux Quantum (SFQ) logic circuits however, experience non-adiabatic bit energies that are consumed during computations. Moreover, it is necessary that these bit energies are set sufficiently higher (normally over 1000-times) than the thermal noise energy k_BT, in order to reduce bit error rates. Contrary to this, the author and his group have demonstrated extremely small bit energies in a superconducting circuit operated slowly and adiabatically, referred to as a quantum flux parametron (QFP).

Until now, the operational parameters of an adiabatic QFP (AQFP) circuit have been clarified[5)], the relationship between AQFP circuit parameters and operating margins verified[6)], the energy consumed experimentally evaluated[7)], and an AQFP logic circuit demonstrated [8)]. The research conducted thus far has established that a circuit utilizing critical dumping junctions with relatively large losses will enable an AQFP circuit with a bit energy of around 170 k_BT to operate at a 5 GHz clock frequency.

Landauer et al., predicted that there was no lower limit of energy required for computing as far as there was no reduction in information entropy accompanied by the computations, resulting in limiting to be minimum k_BTln_2 of energy consumed accompanying the erasing of information[9)]. There have been arguments for and against this threshold but these have yet to be resolved. Our research has investigated the bit energy threshold of an AQFP. The bit energies have been evaluated by computing and circuit operations have been experimentally demonstrated at the AQFP gates by utilizing low loss junctions without shunt resistances[10)].

Figure 1 shows the circuit diagram of the AQFP. A relatively small loop inductance is employed for the purpose of adiabatic operation, driving the circuit at a clock current I_x exhibiting a low-speed rise/fall time. Figure 2 shows the time dependency of the AQFP circuit bit energy utilizing unshunted junctions (I_c=50 μA, β_c ~ 2600) with the rise/fall of the clock. The figure shows that the bit energy reduces inversely to increases in the rise/fall time of clock current I_x. This bit energy is around 1/50th the size compared to that of an AQFP

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circuit utilizing critical dumping junctions. Also, it shows that in cases where the rise/fall time is greater than 1000 ps it is possible to operate with bit energies below the Landauer limit at 4.2 K. Contrary to this is that if the rise/fall time goes below 200 ps, this tends to induce plasma oscillations in the circuit, which rapidly increases the energy consumption (refer to the figure insert shown in Figure 2). It is possible to make computations physically and logically reversible using the AQFP gate investigated by this research. Thus, it is theoretically possible to undertake logic operations below the Landauer limit as was demonstrated by simulation studies in our group. The author and his group have also demonstrated circuit operation with sufficiently small error rates at T=4.2 K by studying the influence of thermal noise on circuit operation [10].

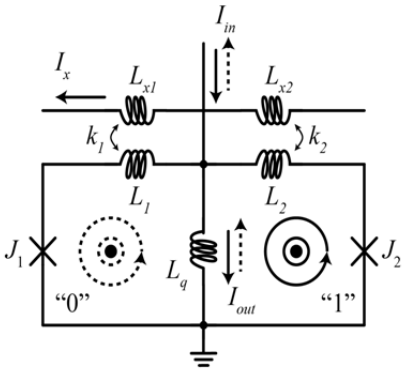

Fig. 1 AQFP gate

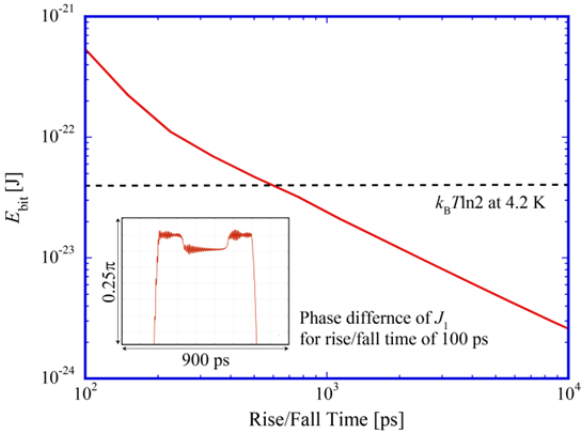

Fig. 2 Time dependency of an AQFP gate with the rise/fall of bit energy clock. Unshunted junction I_c = 50 μA, β_c ~ 2600

Figure 3 shows the low-speed measurement results of 6-stage AQFP logic gate utilizing unshunted junctions. The circuit was fabricated using a standard Nb process (STP2) developed by AIST. The figure shows circuit operation at sufficiently wide operation margins.

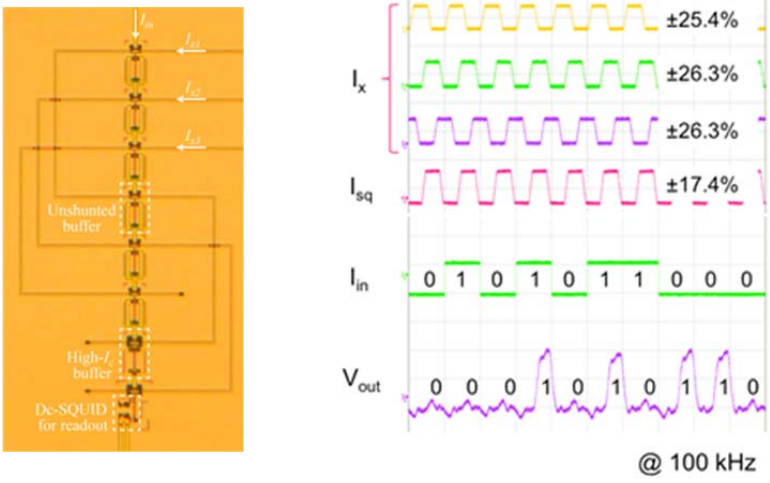

Fig. 3 Demonstration of a 6-stage AQFP gate utilizing unshunted junctions.
(a) Photomicrograph, (b) Low-speed measurement results (Measurement frequency 100 kHz)

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The research highlighted in this article reveals the operation of an AQFP circuit with bit energies less than thermal noise. Whilst future issues are to analyze the relationship of bit energies with changes in information entropy during computation, the author and his group have already begun investigations utilizing AQFP reversible logic gates that do not accompany changes of information entropy. This research is important from a physics point of view and that *"the lower energy limit of computation is to be clarified"*. Also, since reversible computing is relentlessly wasteful during computation itself, it is necessary to consider and investigate the degree to which reversible computation can be adopted in order to engineer and improve energy-efficient computations.

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Feature Article: Superconducting Digital Devices - Development of Small Al-based Multilayered Josephson Junctions and Their Application to Quantum Bits

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Superconducting circuits composed of Josephson Junctions have been researched as potential quantum bit candidates making up a quantum computer[1)]. The majority of Josephson Junctions employed for superconducting quantum bits are required to be submicron-sized. Currently, the mainstream of small junctions are still Dolan-bridge junctions[2)], formed by evaporation techniques using shadow masks on a substrate. However, these junctions are not applicable for use in full-scale integrated circuit fabrication because of an undesirable structure being left behind after the fabrication of the junction as well as an inability to fabricate a crossover cable structure. To fabricate a highly integrated superconducting circuit it is desirable to employ small-multilayered junctions, which have a track record in Nb-based integrated circuit technology. An establishment of process technology is therefore anticipated. The author and his group aim for the establishment of a fabrication process applicable for small-multilayered Josephson Junctions utilizing Al-based superconductor, which exhibits superior quantum bit characteristics.

The fabrication of small Al-based multilayered Josephson Junctions has been undertaken using electron beam lithography, forming small patterns together with a precise Al etching process utilizing a chlorine-based reactive ion etching system. Our group has also been developing a process to form an upper contact to a small junction. This process has involved exposing the junction's upper electrode covered by an insulating layer using a planarization method such as CMP rather than a conventional process that fabricates via-holes by etching. The characteristics of junctions with dimensions of around 1μm, fabricated by employing this new technique have been successfully evaluated[3)]. However, the results from these evaluations have revealed that there is further room for improvement to optimize the contact formation process in addition to periphery processes such as cleaning.

Amongst the issues forming a contact is the CMP processing method, which has been altered and applied only during the planarization of the surface of insulating layer, and then employing a fluorine-based reactive ion etching to expose the junction's upper electrode. Furthermore, after forming the junction and during the cleaning process, changing the resist stripping agent suppressed the loss of Al around the junction.

These improvements have successfully resulted in the fabrication of submicron-sized junctions exhibiting favorable characteristics. Figure 1 shows a cross-sectional TEM image of the Al/AlO_x/Al-based multilayered Josephson Junctions developed in this study. The image confirms the dimensions of the junction to be around 100 nm as planned in the design with sufficiently steep sidewalls and the junction-etch stopped around 40 nm above the tunnel barrier. Figure 2 shows the measured I-V characteristics for the Al-based multilayered Josephson Junctions operating at 300 mK for a 80 nm junction, the smallest fabricated so far. Despite the small dimension, which is smaller than 100 nm, a clear superconducting gap is measurable.

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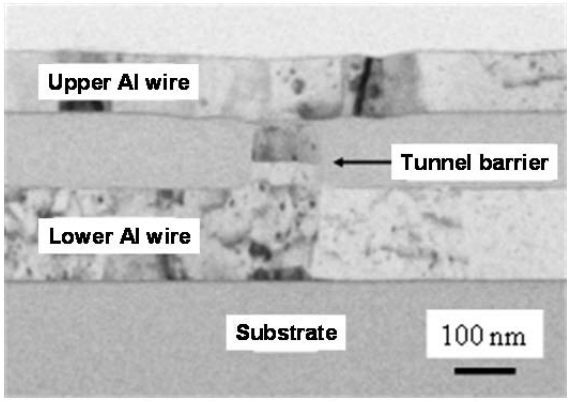

Fig.1 Cross-sectional TEM image of a small Al-based multilayered Josephson Junction

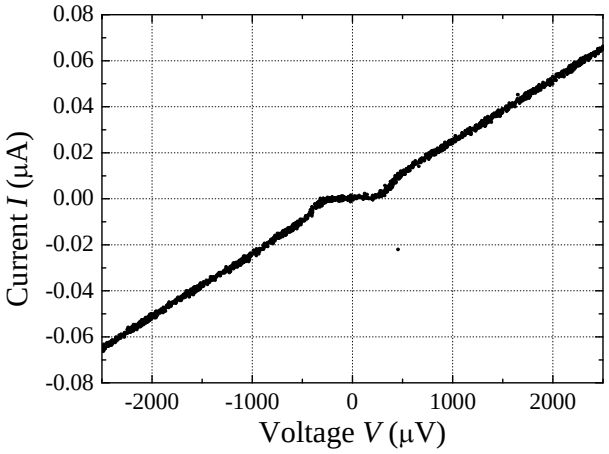

Fig. 2 The I-V characteristics of an Al-based multilayered junction at 300 mK. The junction is 80 nm.

The future plan is to fabricate prototypes and evaluate the characteristics of superconducting quantum bits utilizing these small Al multilayered junctions.

Acknowledgements
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Feature Article: Superconducting Digital Devices
- Integrated Quantum Voltage Noise Source - Creating *Beautiful* Noise

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Although noise is an unpopular issue in both daily life and science/industrial activities, the research taken here is to create "*beautiful noise*" and is introduced herewith.

Noise that is "*beautiful*" varies according to personal perception. From the author's viewpoint, it can be compared to the image of an ideal lady with fair skin (white) and good demeanor (calculable). Additionally, it would be perfect if this were coupled with modesty (low cost).

Figure 1 shows an integrated quantum voltage noise source under development. The key components are a pseudo-random number generator, pulse number multiplier, and a voltage multiplier. All are fabricated using a superconducting single flux quantum (SFQ) circuit and integrated into a single IC chip. The pseudo-random number generator generates a two-value, pseudo-random number sequence of SFQ pulses based upon an M-sequence algorithm. It is well established that during practical use the random M-sequence becomes white noise if the repetition period is made sufficiently long. Because of the weak SFQ pulse, the M-sequence noise can be multiplied using the pulse number and voltage multiplier, enabling the realization of a number of applications. The reason to use "*multiply*" instead of "*amplify*", which is typically used, is to emphasize the fact that the voltage waveform is composed of quantum-superposition of quantized SFQ pulses. This method guarantees the precision calculation of the output noise waveforms. Refer to references 1) and 2) for further details.

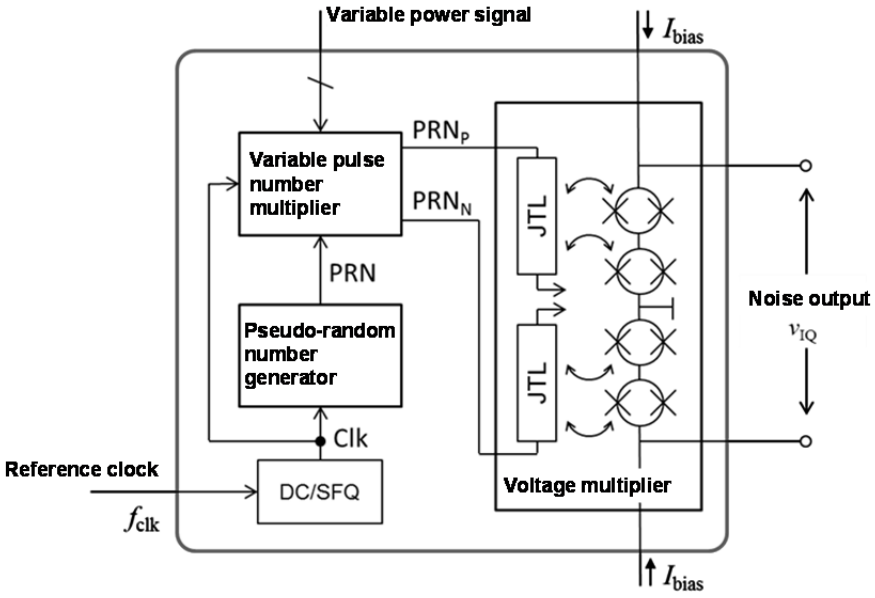

Fig. 1 Block diagram of the integrated quantum voltage noise source

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The National Institute of Science and Technology (NIST) originally invented a quantum voltage noise source utilizing superconductivity. Superconductivity was employed for only the output circuit (the part of voltage multiplier shown in Figure 1). Due to issues attributed to room-temperature electronics equipment, further improvements to their usability and costs are anticipated (figuratively speaking, it's currently a high maintenance lady). The author and his group have proposed an integrated voltage noise source aimed at solving the above-mentioned issues. The analysis of design circuit has been undertaken and the design of prototype circuit component is currently underway.

In conclusion, if the noise becomes beautiful (according to my figure of speech), the question still remains as to how this noise can be utilized. Our target for the time being is set to enhance the performance of a thermal noise thermometer, which will be utilized for temperature standardization and precision measurements. Research is ongoing aimed at a wide range of future applications, including spread-spectrum communications and cryptography, in addition to high frequency noise standardization utilized for the evaluation of high frequency equipment.

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