

# ***Superconductivity Web21***

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## What's New in the World of Superconductivity

(Nov., 2015)

초전도 뉴스 -세계의 동향-

超电导新闻 -世界的动向-

chāo diàn dǎo xīnwén - shìjiè de dòngxiàng-

Yutaka Yamada, Principal Research Fellow  
Superconductivity Research Laboratory, ISTE C



★News sources and related areas in this issue

### ►Power Application

#### 2 - 4 km HTS Cable Plan

**TenneT (10 Sep, 2015)**

TenneT is planning to install 2 - 4 km underground superconducting high-voltage cables as part of the Dutch electricity grid, and determining a suitable demonstration site. At the initial stage, it will only be possible to use superconducting cables in sections of up to 4 km because of nitrogen cooling limitations.

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Superconducting cables are also expensive, costing approximately three times as much as a standard 110 kV or 150 kV cables. Current 150 kV cables require a minimum 12 m-wide strip of soil to dissipate the heat generated. HTSC cables can be placed closer together because they generate no heat, so that a 3 m-wide strip is probably sufficient. Additionally, HTSC cables do not generate any magnetic fields.

HTSC cables are already used on a small scale in other countries, but typically do not form part of the meshed high-voltage grid. In 2009, a 600 m section of HTSC cable was installed in New York, and in 2014 a 1 km-long section HTSC cable replaced a 10 kV medium-voltage line in Essen, Germany. The project to be undertaken by TenneT is much larger, involving cable sections 2 - 4 km long. TenneT CEO Mel Kroon stated, "With this project, we are meeting society's demand to install more high-voltage lines underground." The project is scheduled for completion in June 2019.

TenneT is collaborating with Researchers at Delft University of Technology, University of Twente, the Institute for Science and Sustainable Development (IWO), HAN University of Applied Sciences and Imtech Marine, who will investigate the engineering aspects and the requirements that the cable must meet.

TenneT has also developed the innovative new Wintrack pylon, has applied HVDC technology on a large scale to connect offshore wind farms to the onshore grids. It is planning to use new 66 kV connections to connect future offshore wind farms in the Netherlands. Additionally, the Transmission System Operator (TSO) is leading in the underground installation of high-voltage connections. TenneT is the first TSO to build a 20 km-long section of 380 kV cable, and is investigating further possibilities in this area.

Source: "TenneT to undertake demonstration project for innovative 'super cable'"  
(10 Sep, 2015) News

<http://www.tennet.eu/nl/news/article/tennet-to-undertake-demonstration-project-for-innovative-super-cable.html>

Contact: Press Information Department, [communicatie@tennet.eu](mailto:communicatie@tennet.eu)

## ►Medical Application

### 5 Sets Orders of 900 MHz-NMR

#### **Bruker (17 Sep, 2015)**

Bruker announced five orders for their ultra-high field (UHF) nuclear magnetic resonance (NMR) spectroscopy systems with <sup>1</sup>H proton frequency of 900 MHz or above. These UHF NMR orders are from Europe and Brazil, for NMR research in structural biology, intrinsically disordered proteins (IDPs), membrane proteins, macro-molecular complexes and interactions, cell biology, disease research, as well as in advanced materials research.

The recent orders include three 900 and 950 MHz systems from Brazil, Switzerland and the UK. Professor Fabio C. L. Almeida of the Federal University of Rio de Janeiro (UFRJ) commented, "Having a 900 MHz will have a strong impact on the development of NMR and structural biology in Brazil and Latin America".

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Bruker expects that the Aeon 1.2 GHz systems backlog will be shipped in late 2017 and 2018. Revenue timing for future 1.2 GHz systems depends on further progress in high temperature superconductor (HTS) materials and HTS-based NMR magnet technology.

Source: "Bruker Announces Five Ultra-High Field NMR Orders from Europe and Brazil"  
(17 Sep, 2015) News

<https://www.bruker.com/nc/news-records/single-view/article/bruker-announces-five-ultra-high-field-nmr-orders-from-europe-and-brazil.html>

Contact: Dr. Thorsten Thiel, [thorsten.thiel@bruker.com](mailto:thorsten.thiel@bruker.com)

## **►Electronics**

### **Success in 120 km Quantum Key Distribution from Single-Photon Emitter**

**Fujitsu Limited (28 Sep, 2015)**

The Institute for Nano Quantum Information Electronics (Director: Professor Yasuhiko Arakawa), the University of Tokyo, in collaboration with Fujitsu Laboratories Ltd. and NEC Corporation, announced they have achieved quantum key distribution at a world-record distance of 120 km using a single-photon emitter system.

The new system comprises two key components; high-purity quantum dot single-photon emitter operating in the 1.5  $\mu\text{m}$  band, and an optical-fiber-based QKD system optimized with single-photon emitters. The technology employs individual photons to transmit information, enabling two parties to share a cryptographic key, allowing secure communication between parties. It artificially mixes optical pulses with different intensities, guaranteeing a high level of security by the laws of quantum mechanics.

Another reason behind the success is the QKD system, which is optimized for Single-Photon Emitters using superconducting Single-Photon Detectors. A low-loss interference system optimized for operation at 1.5  $\mu\text{m}$  was demonstrated in the Tokyo QKD Network. A noble superconducting single-photon detector with ultra-low noise characteristic was also attained. The researchers are aiming towards making the QKD system more compact and faster, and rolling out highly secure communications for major urban centers from 2020.

Source: "University of Tokyo, Fujitsu, and NEC Succeed in Quantum Key Distribution from Single-Photon Emitter at World-Record Distance of 120 km" (28 Sep, 2015) Press Release

<http://www.fujitsu.com/global/about/resources/news/press-releases/2015/0928-02.html>

Contact: Dr. Yasuhiko Arakawa, [arakawa@iis.u-tokyo.ac.jp](mailto:arakawa@iis.u-tokyo.ac.jp)

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## ► Basics

### First Superconducting Graphene

#### **The University of British Columbia (8 Sep, 2015)**

Although superconductivity has already been observed in intercalated bulk graphite, superconductivity in single-layer graphene has until now baffled scientists. Physicists from UBC, which include colleagues at the Max Planck Institute for Solid State Research through the joint Max-Planck-UBC Centre for Quantum Materials, have for the first time fabricated the superconducting graphene by coating it with lithium atoms, prepared in ultra-high vacuum conditions and at ultra-low temperatures of 5 K. Coating with lithium atoms enhances the graphene's electron-phonon coupling to the point where superconductivity can be stabilized.

The findings promise a new era of graphene electronics and nanoscale quantum devices, which scientists hope eventually will lead to very fast transistors, semiconductors, sensors and transparent electrodes using graphene.

Source: "First superconducting graphene created by UBC researchers" (8 Sep, 2015) UBC News

<http://news.ubc.ca/2015/09/08/first-superconducting-graphene-created-by-ubc-researchers/>

Contact: Heather Amos, [heather.amos@ubc.ca](mailto:heather.amos@ubc.ca)

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## **Feature Article: Superconducting Digital Devices**

### **- Quantum Annealing System and Superconducting Digital Circuit**

### **Developed by D-Wave**

Mutsuo Hidaka, Chief Senior Researcher  
Superconducting Sensors and Circuits Group  
Nanoelectronics Research Institute  
National Institute of Advanced Industrial Science and Technology

A quantum computer sold by D-Wave Systems in Canada is the focus of recent attention. The system implements quantum annealing algorithms to optimize problem-solving by searching for the global minimum of a function, differing from the familiar quantum gate computers built on prime factorization operations. It is cited that 10 years or more will be required for the realization of a quantum gate computer whilst the very first quantum-annealing system was sold in 2010. Customers include Lockheed-Martin, Google, and NASA, with many commentary articles having been published <sup>1)</sup>.

Quantum annealing solves problems by selecting an optimal solution from a number of potential answers. An example demonstrating optimal problem solving is the well-known traveling salesman problem (TSP). TSP asks the following question; Given a list of cities and the distances between each pair of cities, what is the shortest possible route that visits each city exactly once and returns to the origin city? This question can be solved easily when the numbers of cities visited are small. However, computation volumes increase exponentially with increasing numbers of cities to visit, posing difficulties for classical computers. Even with K computers, the question cannot be answered within a realistic timeframe if the numbers of cities visited exceed 25. A method to efficiently solve this optimization problem is required, especially in a number of fields where Big Data is being generated. A quantum-annealing system offers promise in addressing such computational issues.

Figure 1 shows the quantum-annealing system developed by D-Wave. Although the outline is large in size, the heart of this processor is a chip as shown in Figure 2. This chip is cryocooled to 15 mK by a dilution refrigerator <sup>2)</sup>. The latest chip is based on a fabric of 1152 qubits and contains 128,000 Josephson Junctions (JJ) <sup>3)</sup>. The number of JJs integrated within this chip is the largest amongst superconducting circuits ever built and successfully demonstrated. A qubit utilizes six JJs along with six superconducting ring couplers to allow controllable nearest neighbor coupling. Each superconducting ring coupler employs 2 JJs. These JJs operate as variable inductance devices. Unlike digital circuits, there is no switching to voltage-state. The numbers of JJs operated as variable inductance devices total around ten thousand at most and the remaining 110,000 JJs can operate in the same mode as a digital circuit.

Here, an example is the Digital Analog Converter (DAC), where an individual qubit utilizes 5-units and a single unit for each superconducting ring coupler. Single flux quanta (SFQ) enter into a superconducting loop one by one by switching a JJ to voltage state. This produces a controlled current volume flowing into qubits and superconducting loop couplers necessary for the number of SFQs. The qubit readout employs a Quantum Flux Parametron (QFP) circuit, introduced by Professor Takeuchi of Yokohama National



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University and appears in this feature article. The current in a superconducting loop flows either clockwise or counterclockwise corresponding to the qubit state. A DC-SQUID can then be used to switch this current direction to a voltage-state for readout. Furthermore, the superconducting digital circuit can be used to select a qubit and also be utilized for control as well as readout. The performance of such digital circuits has minimal heat generation and has low noise characteristics. These advantageous attributes lead to qubit's with high noise sensitivity and very small refrigerator-heating budgets, requiring cooling to 15 mK for qubit operation.

The quantum annealing system fabricated by D-Wave employs superconducting Nb, TiPt resistance, and Nb/AlOx/Nb JJ. It has a planarized six-Nb-layer structure. Manufacturing takes place at the 8-inch CMOS line at Cypress, a semiconductor fabrication plant. Light exposure using a KrF Stepper realizes a minimum JJ diameter of 0.6  $\mu\text{m}$  and a minimum wire width of 0.25  $\mu\text{m}$ . This manufacturing process is virtually equivalent to a state-of-art superconducting digital device <sup>4)</sup>.

D-Wave's quantum annealing system utilizes a number of superconducting digital circuit technologies developed up to now. Both qubit performance attributes and their scale-up must be realized to pursue further performance enhancements of the quantum annealing system. To scale-up, digital circuit technology requires exploitation in order to be applicable to quantum annealing applications.



Fig. 1 The quantum annealing system developed by D-Wave Systems  
<http://www.dwavesys.com/d-wave-two-system>

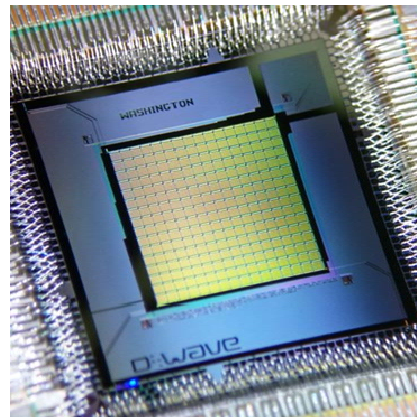


Fig. 2 Latest quantum annealing device  
<http://www.dwavesys.com/d-wave-two-system>

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## Feature Article: Superconducting Digital Devices —100 GHz Superconducting Microprocessor

Masamitsu Tanaka, Designated Lecturer  
Department of Quantum Engineering  
Graduate School of Engineering  
Nagoya University

With a strong determination to fabricate the world's fastest large-scale integrated circuit (LSI), the author's research group aims to exploit the potential offered by superconducting electronics. The integration of superconducting devices will lead LSI to success. Device performance is influenced by a number of factors, which include the high-speed device attributes, addressing issues associated with wiring delays, reducing power consumption, and computer-aided design (CAD) technology.

The notion of utilizing an individual quantized magnetic flux stored within a superconducting loop, as a way of information processing within a logic circuit was conceived in Japan. Following this, Professor Likharev and his research group based at Moscow State University systemized the concept and fabricated a rapid single-flux-quantum (RSFQ) circuit <sup>1)</sup>. High-speed Josephson devices and ballistic signal transmission via lossless, dispersion-free superconducting transmission lines make sub-terahertz operation possible, in principle. However, apart from simple logic circuits such as flip-flops <sup>2)</sup> and shift registers <sup>3)</sup>, LSIs operating at frequencies above 100 GHz have yet to be demonstrated.

In this research, supported by JST ALCA, a fabrication process for the next-generation superconducting LSI with a Josephson critical current density of 20 kA/cm<sup>2</sup> has been developed in collaboration with AIST <sup>4)</sup>, and aimed towards demonstrations of a microprocessor that achieves 100-GHz operation. Making a circular Josephson junctions resulted in 2 % spreads in device characteristics, which is sufficiently small to realize LSIs. A high-precision design technology in a sub-picosecond order have been established by reinforcing circuit parameter and layout design. Also, both the high performance and low power consumption have been successfully balanced by optimizing the power supply voltages in line with the operating speed requirements.

Figure 1 shows the test circuit of an adder comprising the arithmetic logic unit, and the results in high-frequency tests <sup>5)</sup>. Correctness of operations up to approximately 140 GHz were verified. A detailed evaluation of the simple microprocessor incorporating the adder is currently ongoing. Operations performed at around 100 GHz were confirmed with a power consumption of 1 mW. Thus, we have been successfully demonstrating the potential of RSFQ microprocessor competitive to semiconductor-based microprocessors, with 6-times greater speeds and 2/3 lower power consumption compared to the microprocessors which we demonstrated for the first time <sup>6)</sup>.

The research and development of microprocessors will pave the way towards the realization of practical superconducting digital circuit technology for the next generation LSI technology.



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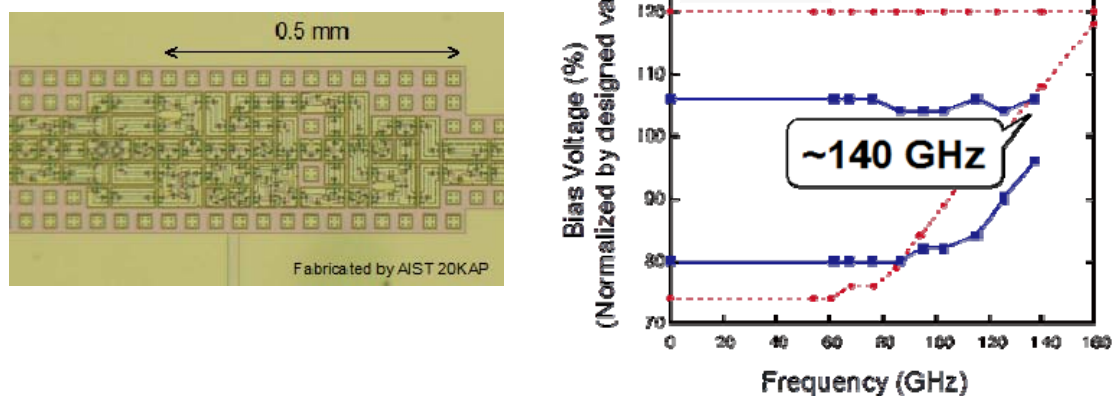


Fig. 1 Microphotograph and high-frequency test results of RSFQ bit-serial adder<sup>5)</sup>

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## **Feature Article: Superconducting Digital Devices -Research for Ultra-Low-Power AQFP Microprocessors**

Naoki Takeuchi  
Institute of Advanced Sciences  
Yokohama National University

Extremely energy-efficient logic circuits are desired for the next generation exascale supercomputers. Here, the author and the research team has dedicated their research efforts for an adiabatic quantum-flux-parametron (AQFP) <sup>1)</sup>, a low-power superconducting logic, in which energy dissipation is significantly reduced due to adiabatic switching operations. This article introduces the latest research towards realizing an ultra-low-power microprocessor utilizing AQFP.

In order to design large-scale digital circuits, an AQFP cell library was built by adopting minimalist design <sup>2)</sup>, in which logic cells are designed by arraying four types of building blocks; buffer, NOT, constant, and branch cells. This design method allows us to build and customize cell libraries for each process much more effectively compared to conventional design methods, where each logic cell is individually optimized. Figures 1(a) and (b) show the layout of the building-block cells and a micrograph of the fabricated logic cells designed by utilizing minimalist design, respectively. The circuits were fabricated using the standard Nb process (STP2), developed by National Institute of Advanced Industrial Science and Technology. Low-speed measurement results of the logic cell tests confirmed wide excitation margins of more than  $\pm 30$  %. Moreover, a circuit comprising of approximately 10,000 buffer gates was fabricated in order to evaluate circuit yields <sup>3)</sup>. Circuit yields for both 1,000-gate and 10,000-gate circuits were measured. The obtained yields resulted in 56 % for the 1,000-gate circuit and 13 % for the 10,000-gate circuit, respectively. By optimizing moat design and cell layout, further improvement in circuit yields can be expected.

In addition, this research team has proposed a magnetically coupled quantum-flux-latch (MC-QFL) <sup>4)</sup> as a low power latch for AQFP logic. The MC-QFL was fabricated using the STP2 process, and wide excitation margins have been measured at low speed. Also, AQFP-SFQ interface circuits, which are necessary for long distance wiring exploiting passive-transmission-lines (PTLs), were demonstrated <sup>5)</sup>. From the above results, physical components including logic cells, latches and wirings have been prepared. Future plans involve constructing digital design environments using EDA and HDL models that comply with the AQFP cell library, aiming for demonstrations of an 8-bit AQFP microprocessor operating in a cryocooler <sup>6)</sup>.

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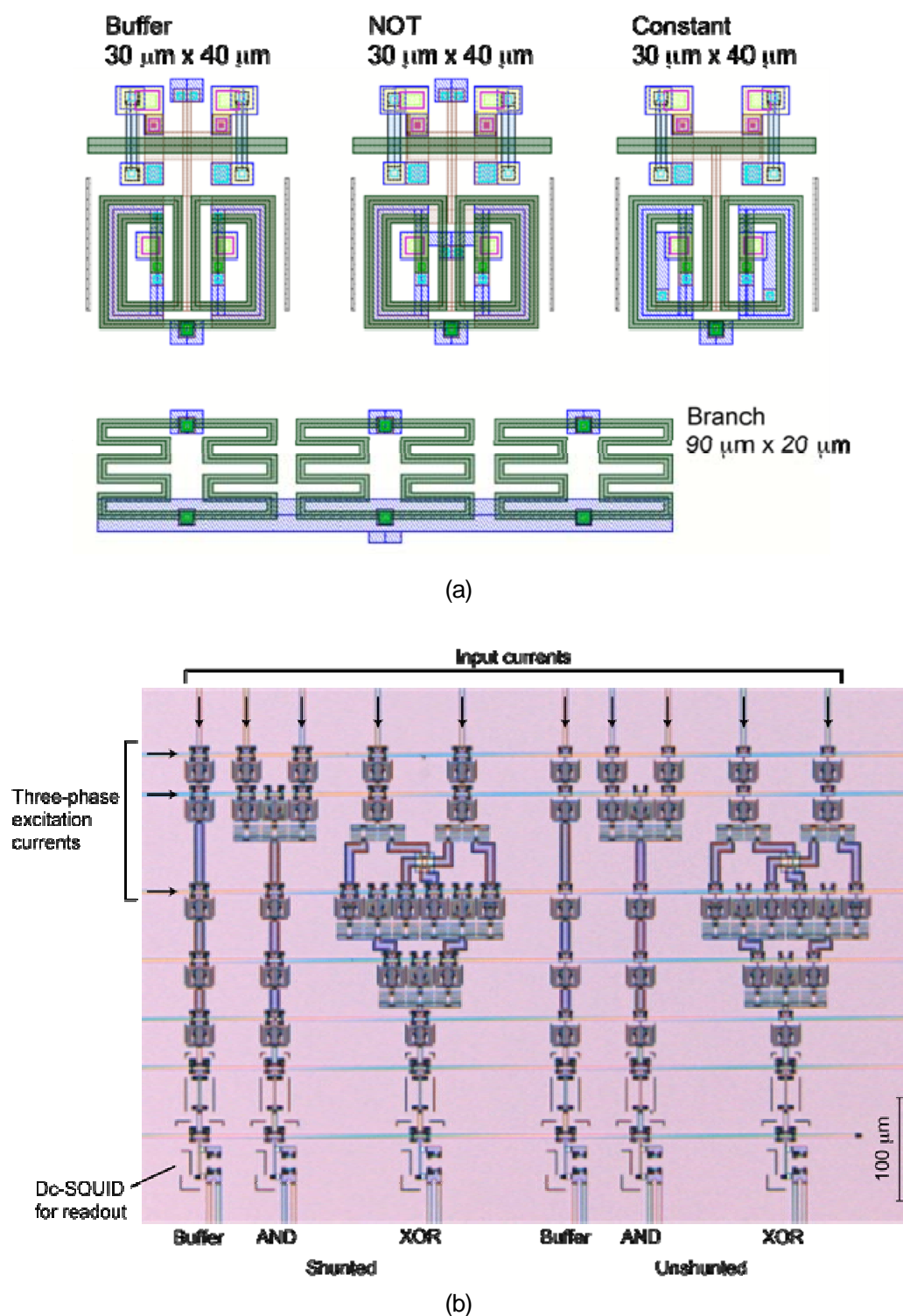


Fig. 1 AQFP logic cells (a) Building block (b) Circuit fabricated for logic cell tests. Two types of the circuit fabricated: circuits with shunted junctions for high-speed operation and ones with unshunted junctions for low-power operation, respectively.

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